Amendments to the Specification:

Please replace the paragraph beginning at line 21 of page 4, with the following:

A non-volatile storage element (NVM) 105 is also connected to system bus 104. NVM 105 is typically implemented with a flash memory card although other implementations may employ an alternative programmable non-volatile element such as a conventional electrically erasable programmable read only memory (EEPROM). NVM 105 typically contains code that is executed by processor 102 immediately following a power-on or hardware reset event. The NVM code typically includes the system's POST/BIOS code. Modifications to a system's POST/BIOS code require either programming the content of NVM 105 or replacing the device with an alternative device. From a cost perspective, it is generally preferable to update or otherwise modify the contents of NVM 105 using an automated process that does not require a technician or other personnel to physically open the system. The present invention contemplates a ~~syste~~ **system** and method for doing so without jeopardizing system security.

Please replace the paragraph beginning at line 1 of page 5, with the following:

In system 100, a bus bridge 108 provides an interface between system bus 104 and an I/O bus 110 to which one or more peripheral devices 114A through 114N (generically or collectively referred to as peripheral device(s) 114) as well as a general purpose I/O (GPIO) port are connected. Peripheral devices 114 may include devices such as a graphics adapter, high-speed network adapter, hard-disk controller, and the like. I/O bus 110 is typically compliant with one of several industry standard I/O bus specifications including, as an example, the Peripheral Components Interface (PCI) bus as specified in *PCI Local Bus Specification Rev 2.2* by the PCI Special Interest Group ~~(www.peisig.com)~~.

Please replace the paragraph beginning at line 10 of page 5, with the following:

The depicted embodiment of SMP **(symmetric multiprocessor)** system 100 includes a service processor 116 connected to GPIO port 112. Service processor 116 is used to provide support for low-level system functions such as power monitoring, cooling fan control, and so forth, hardware error logging, and so forth.